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QCA DESIGN OF SRAM CELL USING REVERSIBLE ADDRESS DECODER

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ABSTRACT

A memory unit is a gathering of capacity cells together with related circuits expected to change data all through the gadget. Memory cells which can be gotten to for data exchange to or from any coveted arbitrary area is called Random Access Memory (RAM). A decoder is an imperative part of memory, for address disentangling and encoding. The sizes of Complementary Metal Oxide Semiconductor (CMOS) transistor continue contracting to build the thickness on chip as per Moore's Law. The scaling influences the gadget execution because of requirements like warmth dissemination and power utilization. A Quantum spot Cellular Automaton (QCA) is another option to CMOS. It offers higher speed, bring down power utilization, and higher thickness. In non reversible doors some measure of energy misfortune is included. Enthusiasm for reversible rationale offers lessened warmth dispersal and expands the speed. It is another transistor less calculation in nanotechnology. In this venture propose a SRAM CELL configuration utilizing Feynman gate based decoder.It gives reversibility and territory minimization. QCA architect instrument has been utilized to approve the execution of reversible decoders.

Keywords- *Quantum Dot Cellular Automata (QCA), SRAM, Reversible Gates.*

I. INTRODUCTION

The measure of Complementary Metal Oxide Semiconductor (CMOS) transistor keeps contracting to extend the thickness on chip according to Moore's Law [1]. In CMOS innovation, its component measure has decreased following a very long while [2]. Then again, several obstructions still exit. This has realized the speedy headway of nuclear plans on the nanoscale. QCA is one of the alternatives in nanotechnologies for FFT based gadget. It is depended upon to finish low zone and power usage and high trading speed.It has no voltage source and the position of electrons chooses the sensible qualities.

QCA cell involve four quantum dots masterminded in square example [3]. Each cell has two electrons which are liberated to entry to close-by spots. Electrons tend to keep farthest division between each other, they live corner to corner to each other as a result of equivalent electrostatic dreadful oblige between them. Cell has two special states, addressed by method of reasoning 0 and basis 1 [4].

Reversible circuits don't lose any information, and it can be make extraordinary yield vector from each data vector. Landauer showed that joules of imperativeness are made for each bit of information lost in view of non reversible figuring; essentialness dispersing would not by any means occur in reversible estimation. In Reversible entryway, there is composed mapping between the data and yield which is not the circumstance with customary premise. Using this reversible method of reasoning we can recuperate commitment from yield and the amount of data lines is equal to number of yield lines.

In this paper a gainful approach to manage examination and blueprint of SRAM with reversible address decoder using Quantum dot Cell Automata. This paper we use the larger part entryways is the fundamental fragment of the QCA circuit execution. The reversible SRAM circuit is laid out and propagation results are poor down using QCA originator instrument. The proposed structure of reversible SRAM required a decreased number of dominant part entryway capacities.

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II. REVERSIBLE DECODER

A powerful way to analyse and design of decoder with reversible NAND gate, which utilizing quantum dot cell automata in nanoscale. This paper we utilize the largest part gate is the principal segment of the QCA circuit execution. The proposed circuit is designed and simulated using quantum dot cell automata designer tool, this test system tool is more helpful for building an intricate info levels. The proposed structure required less number of greater part gate capacities contrasted with past structures.

A. Feynman Gate

Feynman gate is a fundamental reversible gate. It has two sources of info and two yields [6]. To start with yield is same as the information and the other is XOR of contributions as appeared in Fig.2.1

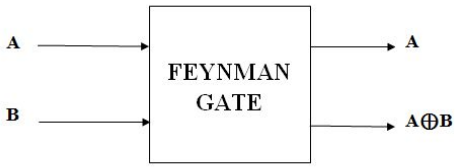

Figure 2.1 Feynman Gate

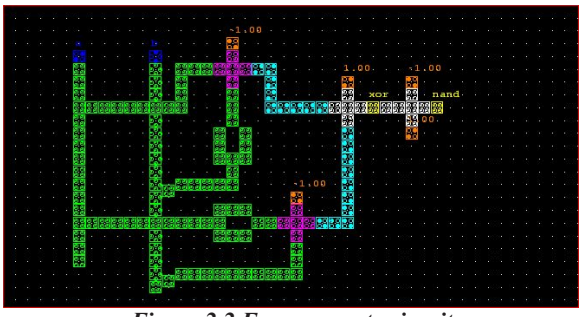

Figure 2.2 Feynman gate circuit

B. Design a reversible decoder in QCA

Feynman Gate based 4 to 16 decoder can be designed in QCA. In this Reversible decoder area can be minimized and it offers a higher speed [7].

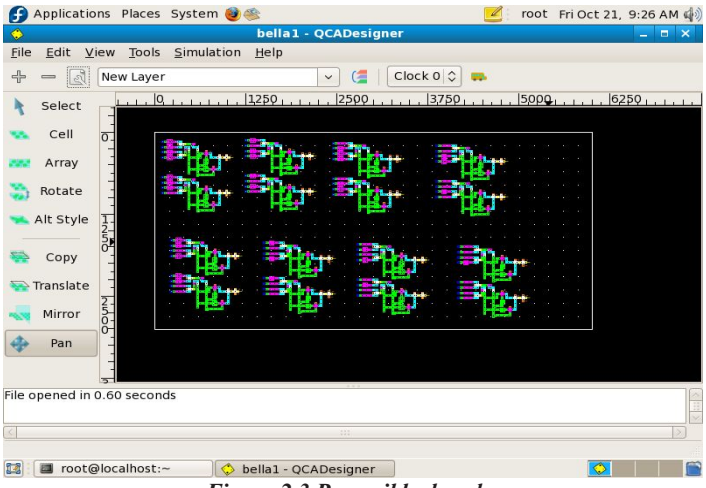

Figure 2.3 Reversible decoder

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III. PROPOSED SRAM DESIGN

A 4-to-16 decoder addresses the 16 SRAM paths which has four tending to lines that can deliver up to 16 SRAM paths. Subsequent to choose the coveted SRAM path, as per the R/W line, 32 bits of information can be composed or perused. The read or write operation from one 32-bit SRAM path is connected as per the way delays and happens at the same clock. The R/W input decides the read or write method of the SRAM. An EN input interfaces with empower the decoder.

Decoders select every unit of memory cell having least deferral. The sensible action of the circuit is as per the following. At the point when the SRAM is chosen by the empower contribution of a decoder (EN), in the event that one SRAM path is chosen by four tending to decoder lines at the same time, then it will be chosen for R/W mode.SRAM will stay idle. If the R/W line is in a high state, written work happens. The R/W line and info information transport must achieve their separate memories amid one clock stage, on the grounds that the memory prepared to compose the info information is embedded in the meantime.

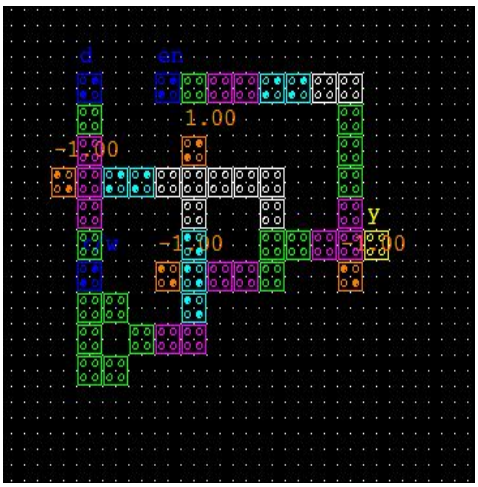

Figure 3.1 Memory Cell

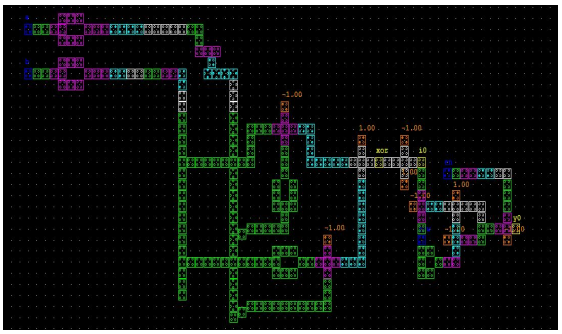

Figure 3.2 QCA Layout of SRAM1(using 2 to 4 reversible decoder)

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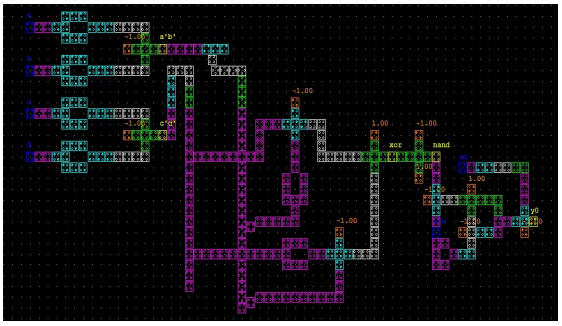

Figure 3.3 QCA layout of SRAM2 (using 4 to 16 decoder)

IV. SIMULATION RESULTS

The output of the SRAM combined with reversible address decoder shown in fig 4.The total simulation time 0.51s.

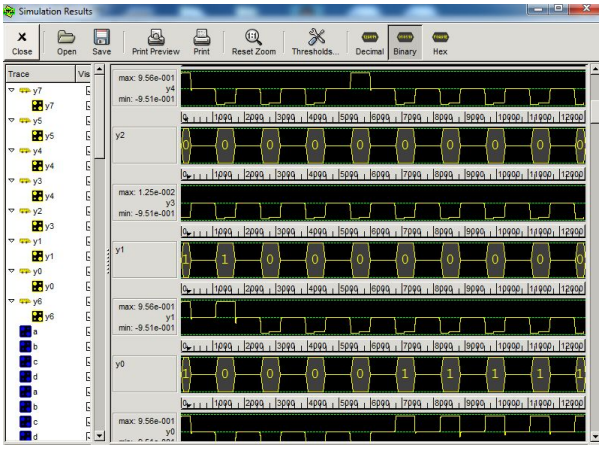

Figure 4.1 SRAM Output

V. COMPARISON RESULTS

The simulation results Cell Count, Area are listed in Table I, Table and II.

Table.1 Comparision Of Reversible Decoder

S.No.	Reversible Decoder	Number of cells	Area(µm)^2
1	2 to 4 decoder	808	2.32
2	4 to 16 decoder	3968	13.79

Table 2 Comparison Of Area

S.No.	SRAM	Number of cells	Area(µm^2)
1	Memory cell	51	0.06
2	SRAM1	1012	4.37
2	SRAM2	4784	14.37

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VI. CONCLUSION

The design under consideration, i,e reversible decoder is said to be an area effective when designed with QCA rather than CMOS. There is an advantage of both low area and power at the same abstraction level, QCA can be seen as one of the promising technologies in near future. However there is still research going on in the inter disciplines of physical implementations and cost effective manufacturing process. High speed decoder is the essential components in fast SRAM[9].The memory cell combined with the reversible address decoder implemented and results can be verified. The proposed SRAM which will be highly delay efficient design

REFERENCES

1. *D.Grier, "The innovation [Moore's law in semiconductor industry]."Computer, vol.39,pp.8-10,Feb 2006.*
2. *Steven C.Henderson,Eric w.Johnson,Jason R Janulis and P.Douglas, "Incorporating Standard CMOS Design process Methodologies into the QCA logic Design Process,"IEEE Transactions on Nanotechnology,vol.3,no.1,March 2004.*
3. *P.Agrawal and B.Ghosh, "Innovative design methodologies in QCA,"Int.J.Circuit Theory Appl.,vol.43, no.2,pp 253-262,2015.*
4. *Heumpil Cho,Earl E.Swartzlander. "Adder and Multiplier Design in Quantum-Dot cellular Automata,"IEEE Transaction on Computers,vol.58,no.6,June 2009*
5. *D.Balobas and N.Konofaos, "Desig of Low Power,High Performance 2-4 and 4-16 mixed logic Line Decoders,"IEEE Transactions on Circuit and Systems II,2015.*
6. *A.N.Bahar,S.Waheed,N.Hossain, "A new appoarch of presenting reversible logic gate in nanoscale, "Springer Plus, vol.4,pp.153-159, 2015.*
7. *Jadav Chandra Das,Debashis De and Tapatosh Sadhu, "A Novel Low Power Nanoscale Reversible Decoder Using Quantum Dot CellularAutomata For Nanocommunication,"Third International Conference on Devices,Circuits and Systems(ICDCS'16),2016.*
8. *M.Awais,M.Vacca,M.Graziano, "QCA check node implementation for LDPC decoders," IEEE Trans.Nanotechnol., vol.12, no.3, pp.368-377,May 2013.*
9. *Moein Kianpour and Reza Sabbaghi-Nadooshan, "A Novel Quantum-Dot Cellular Automata X-bit x 32-bit SRAM,"IEEE Transactions on Very Large Scale Integration(VLSI) Systems vol. 23,no. 3,March 2016.*
10. *K.S.Mahalakshmi,.Hajeri Jayashree H.V,Vinod Kumar Agarwal, "Performance Estimation of Conventional Reversible Logic Circuits Using QCA Implementation Platform",International Confrence on Circuit ,Power and Computing Technologies[ICCPCT], 2016.*